Real time analysis of error statistics and FEC schemes for DPSK transmission at 43 Gb/s

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Abstract

The answers to the demand for bandwidth and reach are channel rates up to 43-Gb/s combined with advanced modulation formats and forward error correcting (FEC) schemes. Due to the very low bit error ratios required in high-speed transmission, computer based FEC code performance simulations can only give estimates. A flexible pattern generator and analyzer utilizing Field Programmable Gate Array (FPGA) technology is presented, which is capable of generating and analyzing optical 43-Gb/s G.709 framed data streams in real time. The programmable platform allows implementing arbitrary functions to analyze data also at very low bit error ratios and is utilized for optimization of active receiver controls as well as for FEC code verification.

1   Introduction

Over recent years the transparent length in high-speed optical transmission systems has been extended through the use of stronger forward error correcting codes and advanced modulation formats, which make use of bipolar signal constellations like differential phase shift keying (DPSK). Both developments allow the signal to pick up more noise as well as signal distortions while maintaining the same level of signal integrity.

Statistical properties of accumulated noise and distortions influence the error distribution. While this fact can be exploited for automatic controls necessary in complex 43-Gb/s DPSK receivers, the performance of FEC codes may suffer: During code design it is often assumed that the optical channel including a hard decision at the optical receiver can be described as a binary symmetric channel (BSC). This model becomes inaccurate when imperfections of the real transmission channel including optical modulation and demodulation are taken into account. These inaccuracies and the resulting influence on error statistics has to be considered during verification of the implemented code.

In this paper an experimental setup is presented that allows for simplified FEC code verification and advanced error statistics measurements even for low bit error ratios. First, a brief overview of impairments relevant to DPSK receiver design and FEC code verification is given in section 2. In section 3, the flexible frame generator and analyzer platform is described in detail. The results obtained in the experiments are highlighted in sections 4 and 5. Section 6 summarizes the obtained findings.

2   DPSK Impairments

Whereas FEC performance has improved recently despite a constant 7 % overhead, the OSNR advantage of DPSK over traditional on-off keying (OOK) comes at an increased complexity in transmitter and receiver components [1]. Notably the delay line interferometer (DLI) in the receiver, which is used to convert the differential phase modulated signal to intensity modulation, requires an accurate setting of the delay. While delay-to-bitrate mismatch does not affect the interference properties of the DLI and also shows only moderate signal degradation, the signal is rather sensitive to delay line frequency offset (an interferometer fundamentally relies on the – exactly – constructive / destructive interference between two optical fields) [2,3]. Since the frequency offset or (in other words) delay line phase tuning is dependent on temperature, laser frequency variation, polarization state etc., it is necessary in a commercial system to employ an active feedback control [4].

This control has to work in parallel with other receiver control loops such as automatic decision threshold control (ATC), tunable dispersion compensation control (TDC), polarization mode dispersion compensation control (PMDC), and even adaptive electronic equalizers, such as feed-forward (FFE) and decision feedback equalizers (DFE). Often, these critical receiver controls use the bit error ratio (BER) derived from a FEC decoder as a feedback signal, mainly because of its cost effectiveness and good correlation to any transmission impairment. While the total number of bit errors provide a measure for the signal distortion, conditional bit errors contain additional information about the intersymbol interference (ISI) from adjacent bits [5,6].

Fast operation of various receiver controls based on BER feedback can be achieved only by taking full ad-

vantage of all statistical properties contained in conditional bit errors which offer distinctive information about specific impairments. However, these properties can be analyzed by computer simulations only at high bit error ratios. The flexible frame generator and analyzer platform presented in this paper utilizes FPGA technology in order to evaluate high-speed 43-Gb/s data streams also at very low bit error ratios. These investigations are particularly needed for DPSK transmission because its performance as well as error statistics change significantly with optical signal-to-noise ratio (OSNR): The perceivable deviation of the probability density function (PDF) of phase noise from Gaussian PDF at low OSNR results in an increased occurrence of multiple errors (especially double errors). Additionally, the relative performance of DPSK compared to OOK decreases from 2.7 dB at high BER to 2.4 dB at BER=10^{-3} [1]. Note that long-haul transmission systems employing FEC are usually operated at high BER / low OSNR. Therefore, FEC codes and receiver control algorithms that use the assumption that accumulated optical noise at the receiver can be approximated by additive white Gaussian noise (AWGN) have to be experimentally verified for DPSK.

3   Experimental Setup

Figure 1 depicts the functional blocks of the setup used for the experiments. Either a Xilinx XC2VP100 FPGA or an ASIC can be used to generate pseudo random bit sequences (PRBS) mapped in G.709 frames with FEC codes. For our tests, we solely used PRBS of the length 2^{31}-1 to properly include inter-symbol interference (ISI).
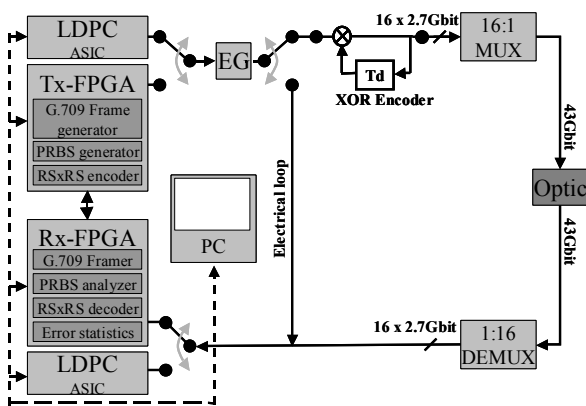

Figure 1 Functional block diagram of the flexible frame generator and analyzer platform.

The data source is followed by an optional error generator (EG) to emulate a BSC channel corrupted with

errors, which can be electrically looped back. This allows the simulation of arbitrary FEC codes much faster for scenarios with low bit error ratios than with conventional methods using software tools on personal computers (PC).

For DPSK transmission, an optional XOR encoder can be switched into the data stream, which is finally multiplexed to 43-Gbit/s and transmitted using the optics setup as described below.

The receive section consists of a demultiplexer followed by another FPGA of the same type or the custom ASIC to detect, decode and analyze the incoming data. The ASIC and the FPGAs are controlled by a PC, which also reads out the data from the analysis generated by the ASIC or the FPGA.
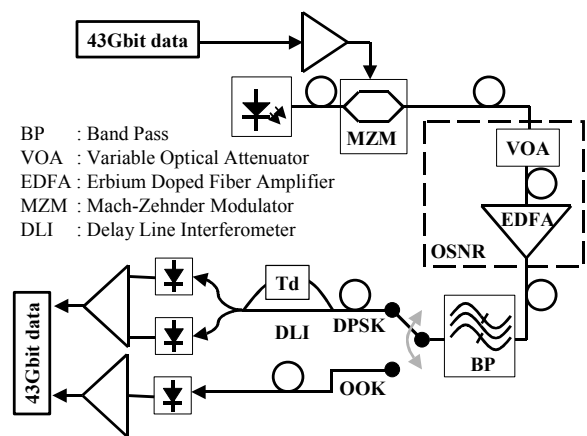
Figure 2 43-Gb/s optics of the flexible frame generator and analyzer platform.

The FPGA architecture allows the implementation and configuration of arbitrary functions. For the experiments, a G.709 frame generator and framer, a PRBS generator and analyzer for variable PRBS lengths as well as an RS×RS FEC encoder and decoder were implemented. Error patterns can be analyzed by the error statistics block in the Rx - FPGA for sequences up to 16-bit including information on multiple errors, as described below.

An additional data connection between the Rx - FPGA and the Tx - FPGA was implemented which allows realizing very complex functions that exceed the capacity of one FPGA by sharing resources between the Rx - and the Tx - FPGA. For even more complex functions, other devices such as ASICs can be connected to the flexible experimental platform. The evaluation of an LDPC FEC code in an ASIC developed by Lucent is part of the results presented here.

Figure 2 highlights the details of the optical transmission path. Laser light at 1550 nm is modulated with the multiplexed (R = 43-Gb/s) data utilizing a Mach-
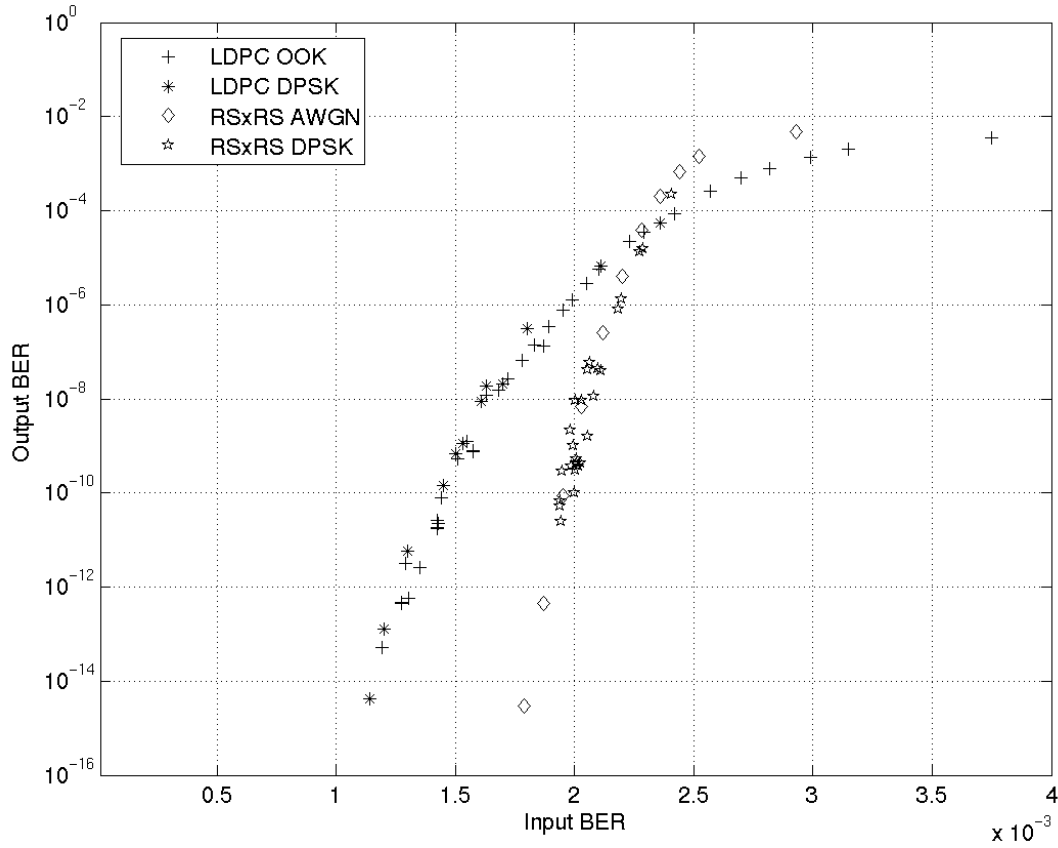
Figure 3 Performance evaluation of FEC codes at low BER for DPSK transmission.

Zehnder modulator (MZM) in push pull configuration biased at either the transmission minimum to generate a DPSK or the quadrature point to generate an OOK encoded optical signal. For DPSK, the driver amplitude is $\sim 2 \times V_\pi$ of the MZM while for OOK, the driver amplitude is $1 \times V_\pi$ to obtain optimum performance. A variable optical attenuator (VOA) in combination with an Erbium-doped fiber amplifier (EDFA), followed by a 2-nm wide optical band-pass filter is used to set the optical signal to noise ratio (OSNR), defined as the ratio of average optical signal power to unpolarized amplified spontaneous emission power in 12.5 GHz optical reference bandwidth.

In case a DPSK encoded signal is transmitted, a DLI with a delay of $T_d = 1/R$ is used to convert the differential phase modulated signal into intensity modulation. The two outputs of the DLI are separately detected by two photodiodes and amplified with a differential limiting amplifier, generating the difference signal. For OOK coded signals, the optical field is detected by a single photodiode followed by a limiting amplifier. In both cases, threshold decision regenerates the data that is demultiplexed and can finally be analyzed by a second receive FPGA or the ASIC.

4 FEC Performance Analysis

Algebraic block codes, especially Reed-Solomon (RS) and Bose-Chaudhuri-Hocquenghem (BCH) codes, fit well to the needs of optical transmission systems, because of their performance at high code rates and the fact that such decoders can be realized with available technology at very high data rates [7,8]. At the given G.709 code rate $r_{709} \sim = 0.937$, the coding gain can be improved by increasing the amount of information covered by one code word. Setting up a product code from two smaller codes is thereby a good method to relax the increasing decoder design complexity and circumvent the degrading performance of those codes for long code words [9].

The G.709 standard uses a 16 times interleaved RS(255,239) code for forward error correction [11]. A G.709 data frame is composed of 4 rows, each consisting of 16 RS code words, i.e. every row has therefore $239 \times 16 = 3824$ information bytes and $16 \times 16 = 256$ FEC overhead bytes. In a structure of 15 rows, a RS×RS product code scheme with an inner RS(255,239+2t) code and a shortened outer RS(240+2t,240) code, with $0 < t < 8$, can be applied in such a way that every information byte is covered by exactly two code words. With a code rate of 3824×15 / (3824×15 +

240×(16-2t) + 239×2t) = 57360 / (61200-2t) >= r_{709}, this structure fits well into the given frame format. In each decoding iteration, the data is first decoded and corrected by the outer decoder and then, in a block-interleaved format, by the inner decoder. No additional information is passed between the decoders. Extrapolations of simulations based on the BSC model have indicated an improvement of up to 2.7 dB for t=5 at a BER of 10^{-16} in terms of coding gain after three iterations for this code compared to the standard RS(255,239) [12]. Due to the low minimum distance t(8-t) bit errors in a 15 × (3824+256)=61200 byte code word can already lead to an uncorrectable result. This is cause for concern that the code might have an error floor above BER 10^{-16}, which cannot be covered by simulations with PCs available today in a reasonable timeframe. Using the programmable frame generator and analyzer platform with an electrical loop setup as described in section 3, the performance of this product code type has been proven down to a BER of $3×10^{-15}$ (see figure 3) without any indication of an error floor.

The constrained resources of FPGAs available today do not allow for implementation of a full 43-Gb/s FEC RS(255,239+2t) × RS(240+2t,240) code. By choosing t=4, both component codes are almost equivalent and the processing in the FPGA is achieved with the implementation of only one decoder-interleaver combination and by serialization of the required six half-iterations. The processed blocks of the 43-Gb/s data stream are handled in real-time, therefore this implementation could be adapted to a full decoder on silicon with ease by merely implementing the same design six times.

The setup shown in figure 1 was used to evaluate the FPGA implementation of the RS(255,247) × RS(248,240) code under the conditions of 43-Gb/s optical DPSK transmission. The measurement results depicted in figure 3 show no major difference between the BSC model and optical DPSK transmission.

The second FEC code evaluated within the scope of this project was a low density parity check (LDPC) code, a type of code well known for its superior performance [10]. Utilizing a bit-flipping algorithm, the LDPC structure allows for a very low power consumption design at 43-Gb/s with low decoding latency. Covering one G.709 row with 30592 information bits at a code rate of $r_{LDPC} \sim= 0.937 >= r_{709}$ makes this non-interleaved systematic code a good replacement candidate for the standard RS code. Figure 3 shows the results from measurements obtained with optical DPSK transmission in a setup as described in section 3. The OOK LDPC measurements in this figure are added for comparison and were obtained with a setup using a former version of the same LDPC codec at 10.7-Gb/s.

5 Active DPSK Receiver Control by Advanced Error Statistics Analysis

The benefit of using powerful FEC codes is that high-speed transmission systems can be operated at higher BER, i.e. tolerate a lower OSNR. Active receiver controls can then be implemented using the cost efficient method of BER estimation from corrected errors out of FEC decoders as feedback signal.

If the DLI as additional component in a DPSK receiver is also controlled by BER feedback, care has to be taken of the fact that controls using this same type of feedback do not interfere. This is important during the startup phase where several receiver controls have to converge quickly to their optimum. Utilizing statistical properties of the bit errors giving more feedback information can significantly contribute to minimize the startup time: For the DLI control, advantage can be taken of the fact that in DPSK transmission errors tend to occur in pairs, especially at low OSNR [13]. An intuitive explanation of these DPSK characteristics is given below.
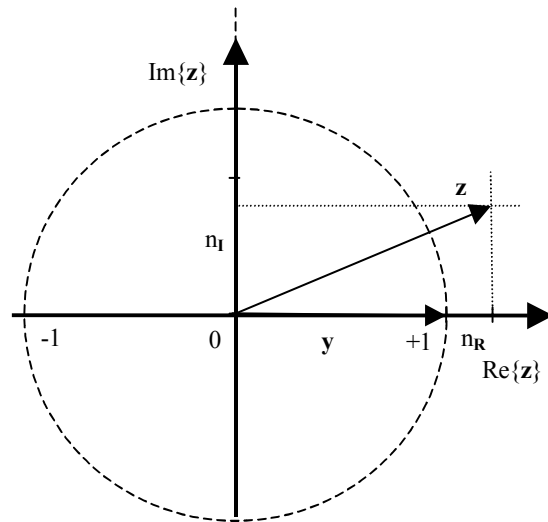
Figure 4 Complex baseband representation of **z**.

The plane in figure 4 depicts the complex baseband representation of the binary PSK signal *z* corrupted by complex noise **n** at the sampling instants:

$$\mathbf{z}(k) = \mathbf{y}(k) + \mathbf{n}(k),$$
$$\underline{n}(k) = n_R(k) + j \cdot n_I(k), \ y(k) \in \{-1;+1\}$$

Since the information is carried in the phase of the signal,

$$\phi_y(k) \in \{0, \pi\},$$

the noise statistics is determined by the probability distribution function of the phase noise:

$$\phi_n(k) = \arctan\left(\frac{n_I(k)}{1 + n_R(k)}\right)$$

For the particular case of complex Gaussian noise the PDF of the phase noise is shown in figure 5 for three levels of optical signal-to-noise ratio. For comparison a Gaussian distribution is shown in addition.
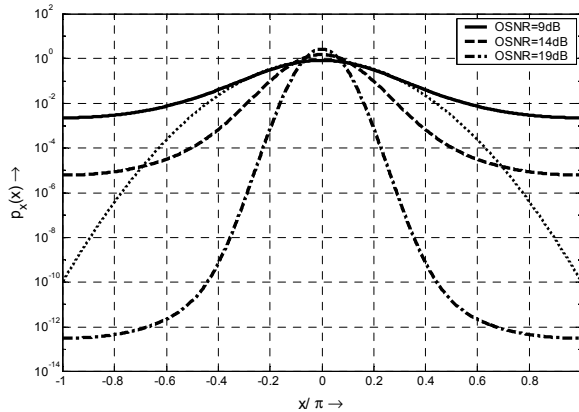
Figure 5 Phase noise distribution function for different OSNR values. Gaussian distribution (dotted) is plotted for OSNR = 9dB.

Demodulation is achieved by taking the phase difference of consecutive bits. For the sake of simplicity we assume the signal phase for both bits to be 0, so that the decision variable is composed by

$$d(k) = \phi_n(k) - \phi_n(k-1).$$

When $d(k)$ is between $-\pi/2$ and $\pi/2$, the decision is correct otherwise an error occurs. It can be seen in figure 6 that the probability density between phase values $\pi/2$ and π remains high for low OSNR, resulting in higher bit error ratios and also higher occurrence of consecutive errors as explained in [13].

Monte-Carlo simulations done prior to the experimental verification support the fact that DPSK transmission will generate a higher rate of double and multiple errors, defined as two or more consecutive error occurrences for a given BER compared to standard OOK.

Furthermore, simulations showed that the ratio of double error probability to single error probability (P_{err2} / P_{err1}) changes with DLI tuning exhibiting distinctive characteristics (two minima, one local maximum). Compared with the curve of the single BER (one minimum) double errors yield additional information that e.g. could be used to do a faster sweep while searching for the initial optimum in the startup phase.
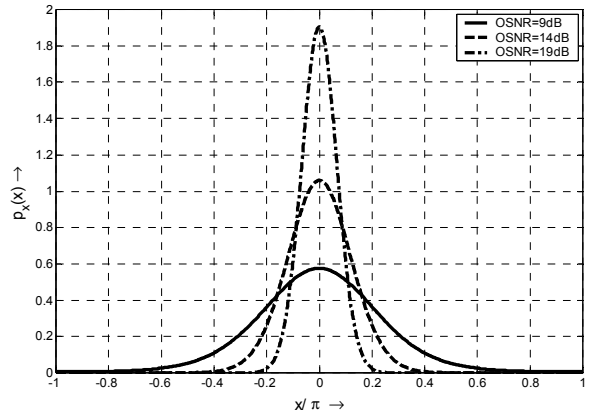

Figure 6 Convolution of noise distribution function for different OSNR values (modulo 2π reduced).

As in existing systems only single bit errors are summed up, measurement of double errors was done using the flexible FPGA setup. The FPGA was programmed to count single, double, triple, etc. errors. Results were transmitted to the host computer after each measurement interval. Measurements were done for various OSNR values, both for single error probability (P_{err1}) and double error probability (P_{err2}).
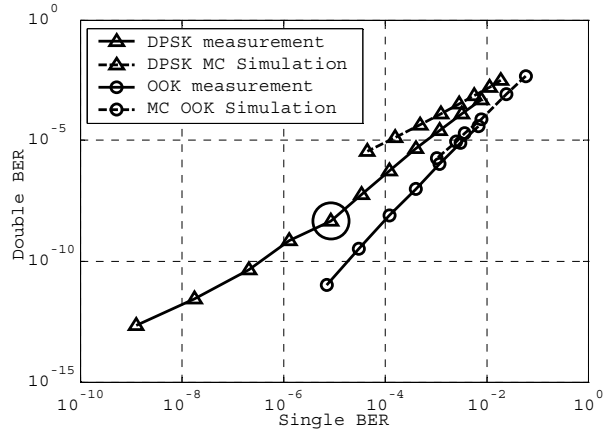
Figure 7 Double BER as a function of single BER 43-Gb/s NRZ DPSK and OOK. The marked data point corresponds to the values in figure 8.

Figure 7 shows the double error probability as a function of the single probability for different OSNR values derived by measurement and Monte-Carlo simulation for OOK and DPSK transmission. Both simulation and measurement confirm the higher occurrence probability of double errors for DPSK compared to standard OOK transmission.
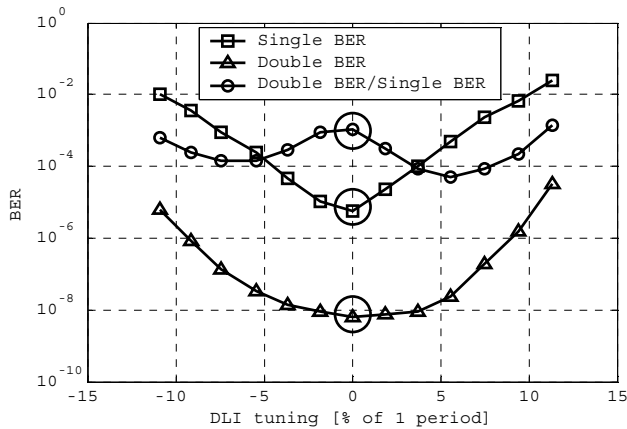
Figure 8 Single BER and double BER over DLI tuning for 43-Gb/s NRZ DPSK.

Figure 8 shows the DLI phase offset from $-\pi/6$ to $+\pi/6$ relative to the performance optimum at zero offset as a function of single error probability (P_{err1}), double error probability (P_{err2}), and double error to single error probability (P_{err2} / P_{err1}) derived from the experiment. The marked data points at zero DLI offset correspond to the marked point in figure 7.

The distinctive characteristics of P_{err2} / P_{err1} as described above can be seen clearly in figure 8. With this experimental verification of theory and simulation it is possible to employ double errors in DPSK receiver control algorithms as a distinct feedback signal.

6   Summary

In this paper an experimental setup based on FPGAs was presented which is used to generate and analyze 43-Gb/s data frames in real time. The programmable structure of FPGA allows for the flexibility to implement arbitrary functions very efficiently compared to an ASIC, which is particularly important for proof of concept demonstrations prior to a costly and time consuming ASIC development. In particular, this FPGA setup was used to verify two FEC codes under DPSK transmission at low bit error ratios and to measure DPSK specific error statistics. As such tasks cannot be accomplished by computer-based simulations in a reasonable timeframe, this flexible platform has emerged as a valuable tool also for future projects.

7   Acknowledgement

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