Taxonomy of Dynamic Power Saving Techniques in Fixed Broadband Networks

Ralph Schlenk[1], Christoph Lange[2], Heiko Lehmann[2], Ron Vleugel[1]

[1] Alcatel-Lucent Deutschland AG, Thurn-und-Taxis-Straße 10, 90411 Nürnberg, Germany
[2] Deutsche Telekom AG, Telekom Innovation Laboratories, Winterfeldtstraße 21, 10781 Berlin, Germany

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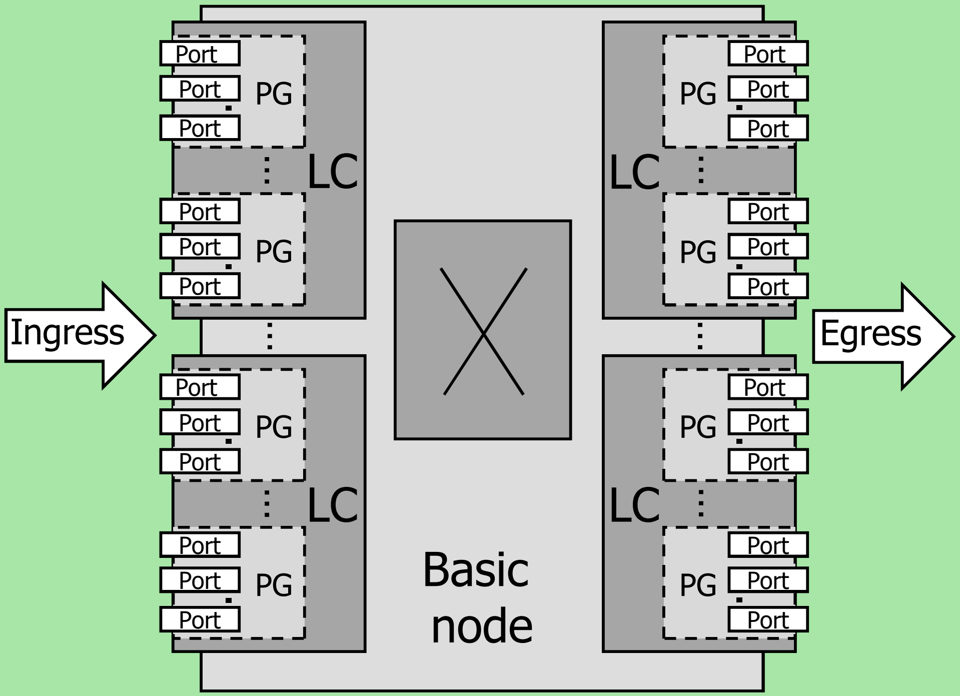
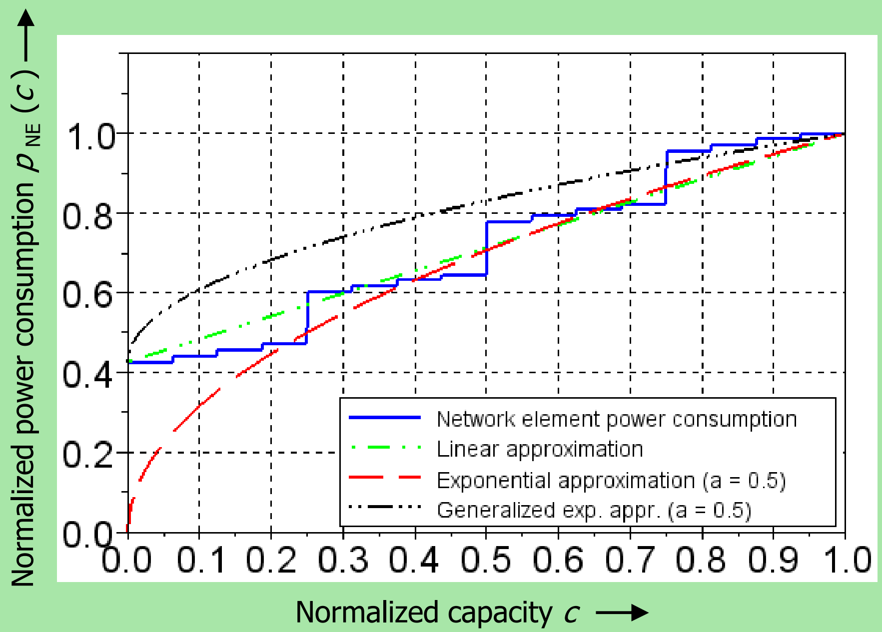
INTRODUCTION
GENERIC NETWORK ELEMENT MODEL





Lange, C.; Schlenk, R.; Lehmann, H.: Network Element Characteristics for Traffic Load Adaptive Network Operation. In: *13. ITG-Fachtagung Photonische Netze*. Leipzig, 07.–08. Mai 2012.

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Dynamic aspects of load-adaptive networking

Network reconfiguration time characteristics

Measurements and results

Conclusion

CLASSIFICATION

Categories

Architectural level
- Subsystem (devices, components, memory)
- System (network elements)
- Network

Timescale
- Intra-packet (less than 10 µsec)
- Intra-flow (10 µsec – 10 sec)
- Inter-flow (10 sec to several min)

Approach
- Rate adaptation
- Sleeping
- Energy-aware data/traffic control

POWER-SAVE TECHNIQUES
TAXONOMY AND ACTIVATION TIMES

Approach	Subsystem			System		Network		
Rate Adaptation	Dynamic voltage and frequency scaling	CPU P-states	10-100 μs	DSL L2 mode	<1 s			
		Memory DVFS	<100 μs	Ethernet RPS	20 ms			
Sleeping	CPU C-states (C1, C2)		10-100 ns	DSL L3 mode	<3 s			
	CPU C-states (C3)		50 μs	PON dozing	1 μs			
	DRAM power-down		<10 ns	PON fast sleeping	<200 μs			
	DRAM self refresh		<1 μs	PON deep sleeping	–			
	CMOS clock gating		10 ns	EEE low-power idle	1-25 ms			
	CMOS clock and power gating		5 μs					
	FPGA suspend techniques		<100 μs					
Energy-aware data/traffic control	CPU idle core "hotplug"		5 ms	Ethernet background traffic buffering	5-20 μs	Energy-aware routing	Interface shutdown	>10 s
	Power-aware virtual memory		<1 μs				Line card shutdown	> 30 s
							Chassis shutdown	minutes
							Protocol conver-gence	n/a

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RECONFIGURATION TIME
SERIAL SWITCHING OF COMPONENTS

Analytical formulation

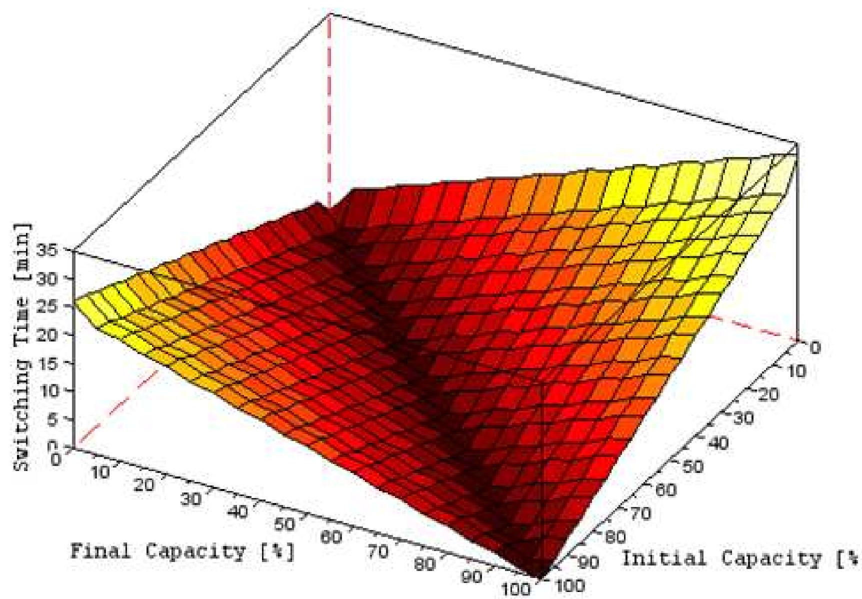
- Activation times (switching on)

$$T^{\mathrm{S}}_{\mathrm{NE\,ON}}(C_{\mathrm{in}}, C_{\mathrm{fi}}) = T_{\mathrm{C_{ON}}} + \sum_{i=1}^{n_{\mathrm{LC_{ON}}}} T_{\mathrm{LC_{ON\,\mathit{i}}}} + \sum_{j=1}^{n_{\mathrm{PG_{ON}}}} T_{\mathrm{PG_{ON\,\mathit{j}}}} + \sum_{l=1}^{n_{\mathrm{P_{ON}}}} T_{\mathrm{P_{ON\,\mathit{j}}}}$$

- De-activation times (switching off)

$$T^{\mathrm{S}}_{\mathrm{NE\,OFF}}(C_{\mathrm{in}}, C_{\mathrm{fi}}) = T_{\mathrm{C_{OFF}}} + \sum_{i=1}^{n_{\mathrm{LC_{OFF}}}} T_{\mathrm{LC_{OFF\,\mathit{i}}}} + \sum_{j=1}^{n_{\mathrm{PG_{OFF}}}} T_{\mathrm{PG_{OFF\,\mathit{j}}}} + \sum_{l=1}^{n_{\mathrm{P_{OFF}}}} T_{\mathrm{P_{OFF\,\mathit{j}}}}$$

Exemplary result



The capacity differences determine the switching times.

RECONFIGURATION TIME
PARALLEL SWITCHING OF COMPONENTS

Analytical formulation

- Activation times (switching on)

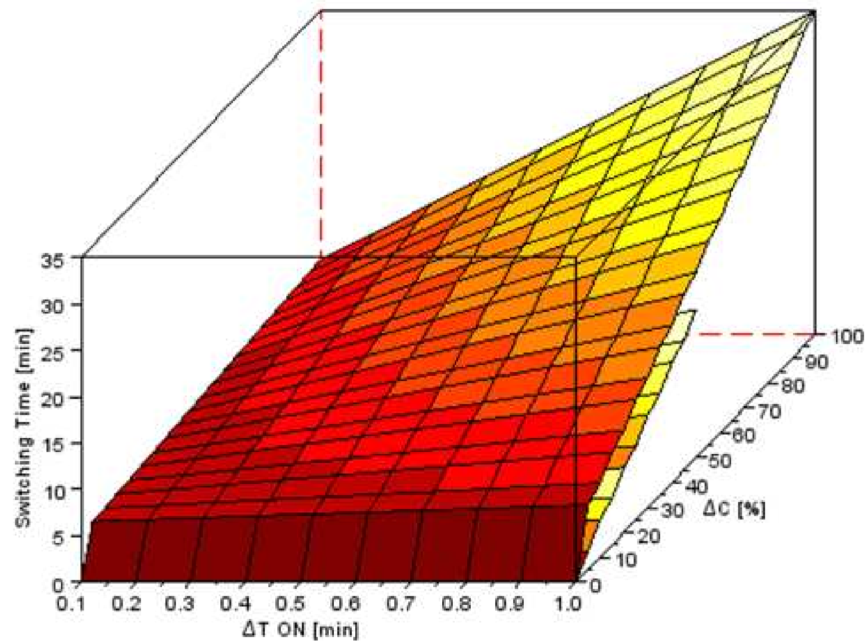
$$T^{P}_{\mathrm{NE\,ON}}(C_{\mathrm{in}}, C_{\mathrm{fi}}) = T_{C_{\mathrm{ON}}} + T_{LC_{\mathrm{ON}}} + T_{PG_{\mathrm{ON}}} + T_{P_{\mathrm{ON}}} + \ldots$$
$$\ldots + \Delta T_{\mathrm{ON}}(n_{LC} + n_{PG} + n_{P})$$

Parameter accounts for additional organization effort

- De-activation times (switching off)

$$T^{P}_{\mathrm{NE\,OFF}}(C_{\mathrm{in}}, C_{\mathrm{fi}}) = T_{C_{\mathrm{OFF}}} + T_{LC_{\mathrm{OFF}}} + T_{PG_{\mathrm{OFF}}} + T_{P_{\mathrm{OFF}}} + \ldots$$
$$\ldots + \Delta T_{\mathrm{OFF}}(n_{LC} + n_{PG} + n_{P})$$

Exemplary result



Capacity differences and ΔT determine the switching times.

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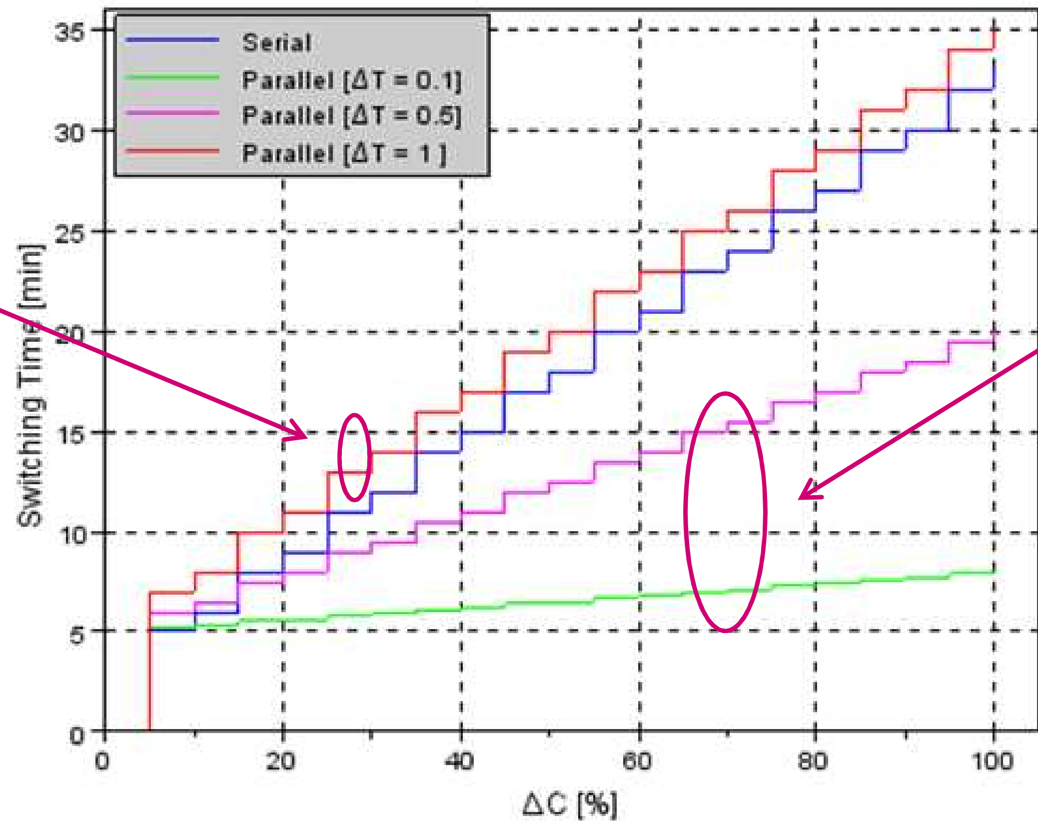
RECONFIGURATION TIME
COMPARISON OF SWITCHING STRATEGIES

High ΔT:

Parallel switching requiring larger time



Low ΔT:

Parallel switching requiring smaller time

Additional processing organization time ΔT is critical.

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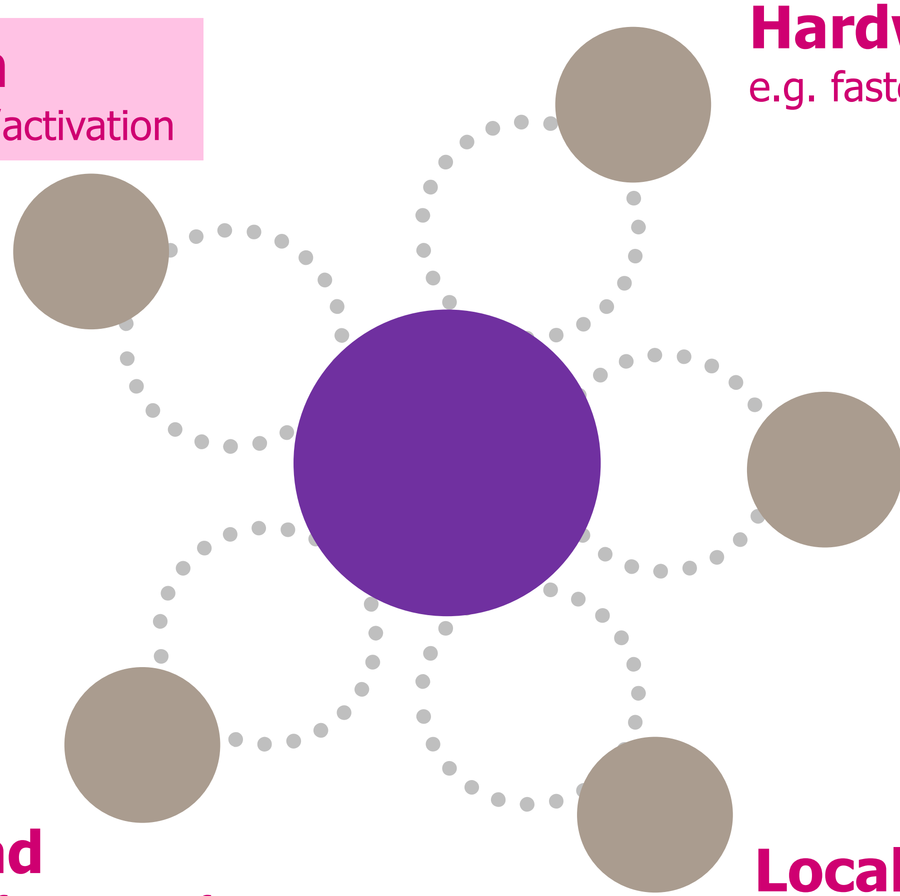
IMPROVING ACTIVATION TIMES
DESIGN PRINCIPLES

Parallelization
e.g. parallel download/activation

Hardware recovery
e.g. faster resynchronization

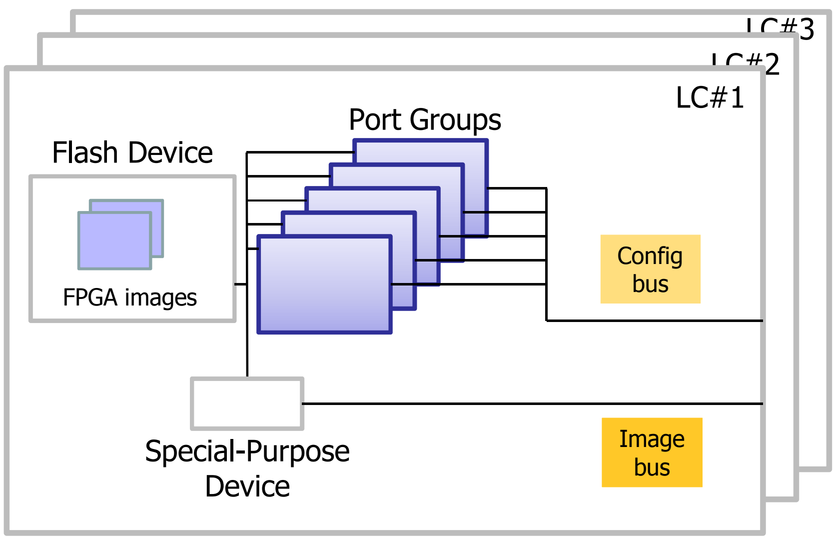


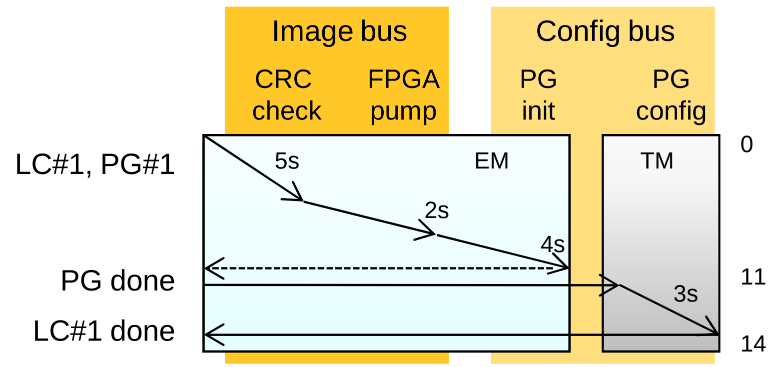
Software recovery
e.g. OS boot time reduction

Fetch-ahead
e.g. essential configurations first

Local persistency
e.g. local configuration storage

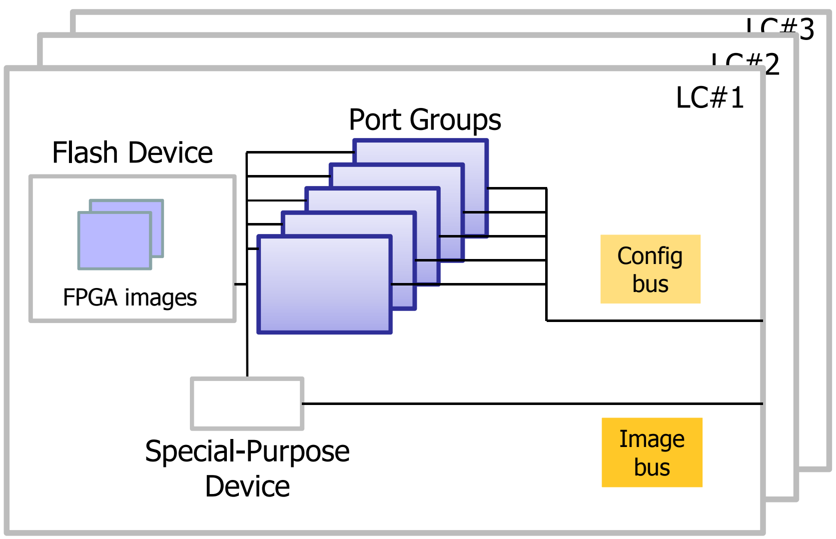
IMPROVING ACTIVATION TIMES
EXAMPLE: LINE CARD ACTIVATION (1)

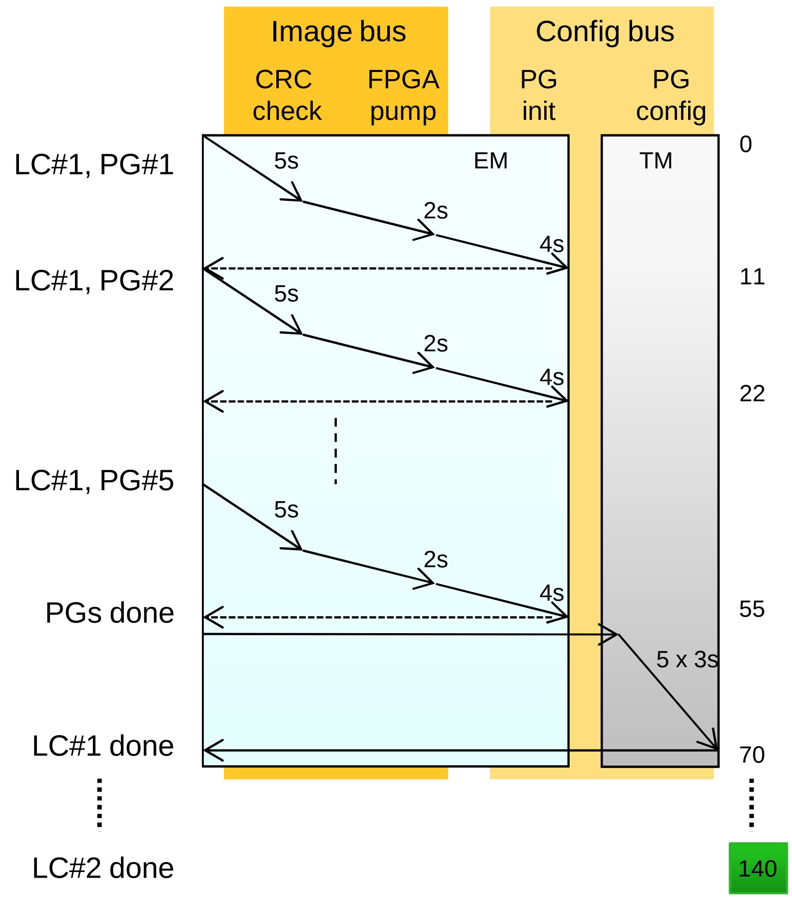




- Line card (LC) with several port groups (PG)
- Two hardware busses (image bus, config bus)
- Two software processes
  - Equipment management (EM)
  - Transmission management (TM)

IMPROVING ACTIVATION TIMES
EXAMPLE: LINE CARD ACTIVATION (2)





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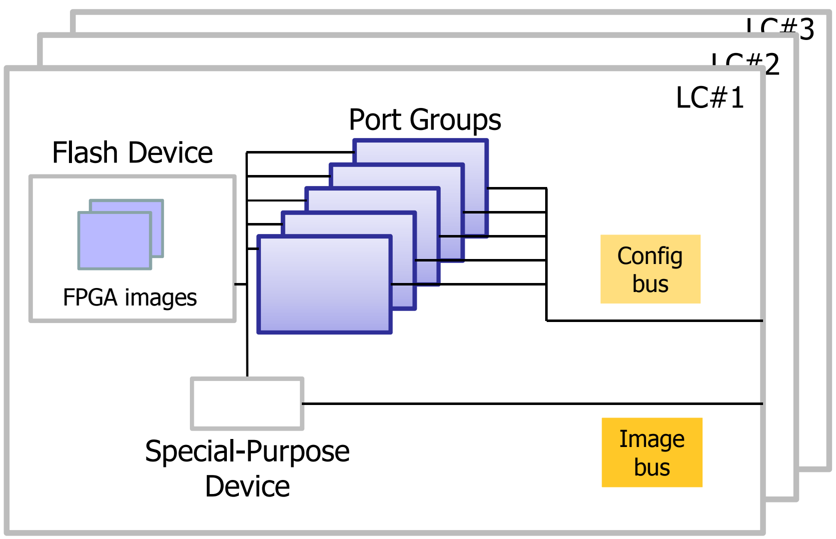
IMPROVING ACTIVATION TIMES
EXAMPLE: LINE CARD ACTIVATION (3)



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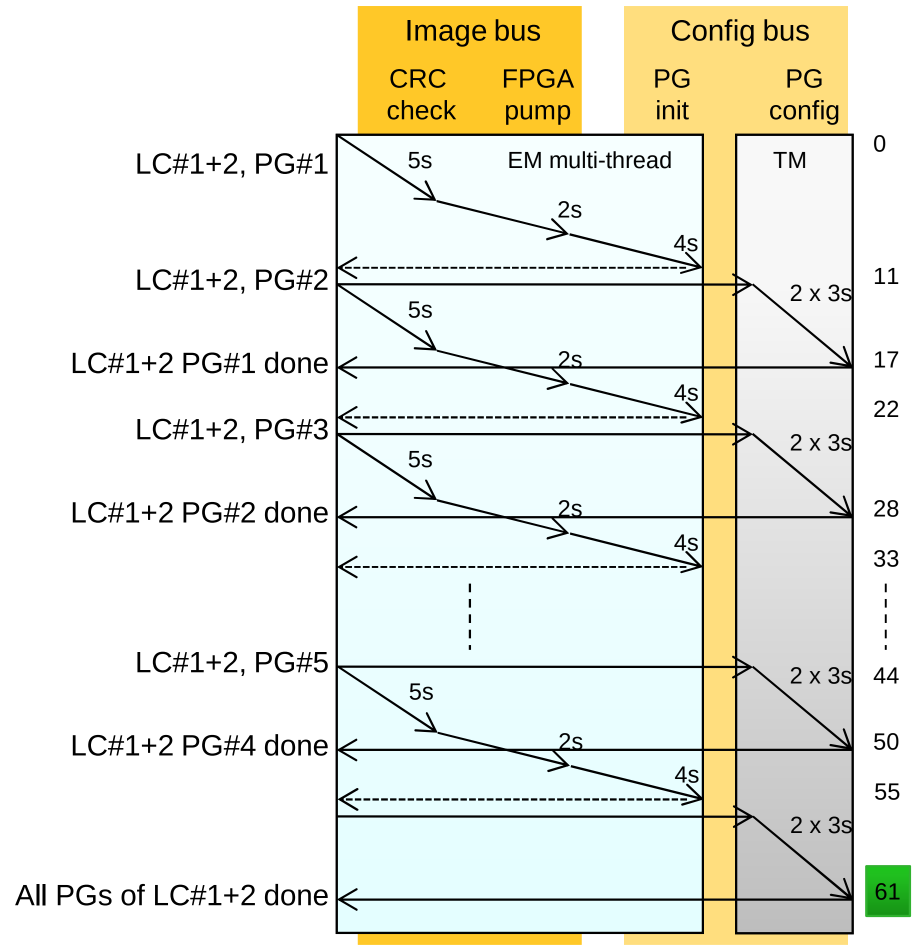
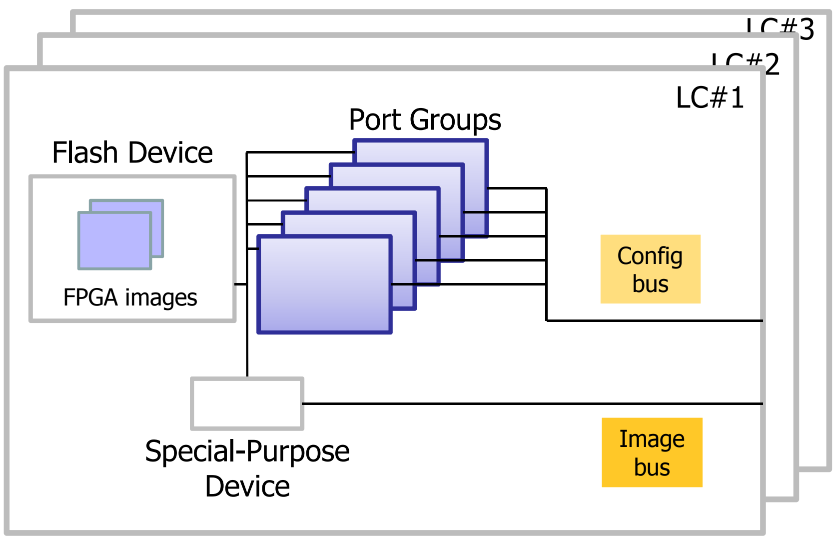
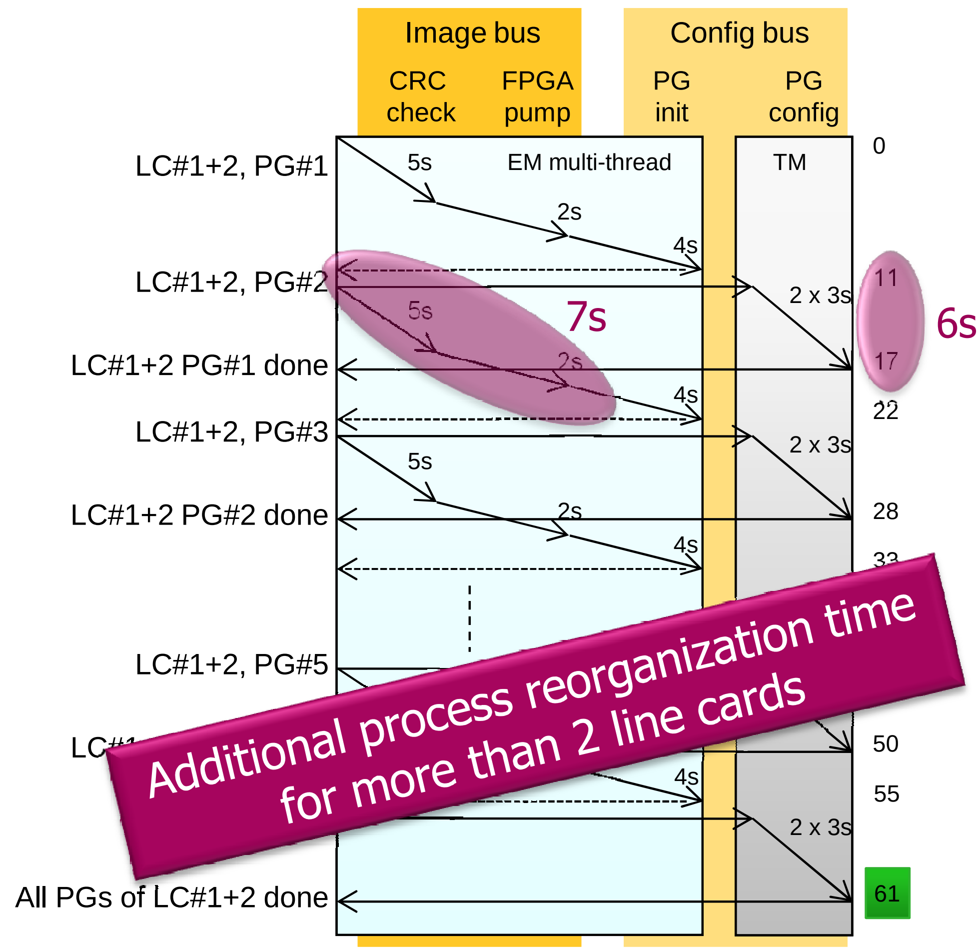


IMPROVING ACTIVATION TIMES
EXAMPLE: LINE CARD ACTIVATION (4)



- Line card (LC) with several port groups (PG)
- Two hardware busses (image bus, config bus)
- Two software processes
  - Equipment management (EM)
  - Transmission management (TM)



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CONCLUSION

Taxonomy	• Categorization of power management techniques according to their temporal properties • Network-level technologies most critical with respect to network performance degradation → Coordination required, e.g. by an energy-aware control plane
Model	• Modeling of network resource activation processes → Extension of the network element power-vs-capacity model • Evaluation of serial and parallel switching strategies
Optimization	• Analysis of a current-generation OTN network element • Serial line card activation process optimized (from 140 sec to 61 sec for two line cards) • Challenges observed when software process split does not match hardware partitioning

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